Approved 12/1/04 JPL

Specification Amendments

Please amend the paragraph starting on page 7, line 17 and continuing to page 9, line 3 as follows:

FIG. 1 further shows that a signal clk1 is used as a clock input to the D flip-flop circuits 102, 104, 106 and 108, the D flip-flop circuits 132, 134, 136 and 138 and the D flip-flop circuits 242, 244, 246 and 248. A signal clk2 may be used as a clock input to the counter 112 and the D flip-flop circuit 114. In one example arrangement, the signal clk1 may be a 100 MHz clock signal and the signal clk2 may be a 400 MHz clock signal. Other arrangements for the clock input frequency are also possible. The use of a 100 MHz clock signal and a 400 MHz clock signal allows 4 pieces of data to be input for every 100 MHz clock cycle. Stated differently, the IO test data comes into the chip at 100 MHz and gets tested at 400 MHz. Based on operations of the D flip-flop circuits, the multiplexors and the clock signals, the data inputs to the D flip-flop circuits 222, 224, 226 and 228 may pass through the output driver circuit 116 and may be captured by the inbound D flip-flop circuits 122 and 124. This is the loopback of the data from the output driver circuit 116 to the D flip-flop circuits 122 and 124. The D flip-flop circuits 122 and 124 may be clocked by the strobe signals stb and stbb, which may operate at 200 MHz to capture the data. Once all four signals (corresponding to that originally provided within the D flip-flop circuits 222, 224, 226 and 228) have been captured in the 8-latch circuit 126, the data may be transmitted to the inbound D flip-flop

circuits 132, 134, 136 and 138. The next clock edge of the signal clk1 may load the data into the core 200. That is, the D flip-flop circuits 132, 134, 136, and 138 bring the data back to operating at 100 MHz. At this point, the scan load enable (loaden) signal may be asserted and the data may be shifted out. That is, data may be shifted out from the D flip-flop circuit 248 as the signal scan_input(next pad). This signal scan_input (next pad) may be compared against the original data that was loaded into the D flip-flop circuits 222, 224, 226 and 228. The signal scan_input (next pad) may be used to determine whether a defect occurs within the chip and, more particularly, whether a defect occurs within the output driver circuit 116. That is, the signal scan_input (next pad) may be observed externally to determine whether a defect occurs.

Please amend the paragraph starting on page 13, line 5 and continuing to page 13, line 17 as follows:

Once the data has been captured in the inbound D flip-flop circuits 242, 244, 246 and 248, the data may be compared with the original data using the XOR circuits 252, 254, 256 and 258. This may occur in the Compare state 312. On the other hand, if the chip is being debugged, then the state machine may enter a Shift mode 316 to scan out data. This selection of the modes 312 and 316 may be accomplished by using a test register that controls the next state selection (between the Compare mode 312 and the Shift mode 316). If in the Shift mode 316 ~~312~~, the chip may operate to shift (or clock) the data until all the data may be shifted out through the scan chain. The state machine may remain in the Shift mode until a shift_done signal is asserted.